UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,207	12/18/2001	Reza-Ur Rahman Khan	1875.1640000	7969

7590 03/16/2004

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Suite 600
Washington, DC 20005-3934

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,207	KHAN ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *28-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-14-03, 7-2-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants' remarks filed November 14, 2003.

Claim Objections

The objection to claim 18 has been withdrawn due to the amendment filed.

Claim 8 is objected to because of the following informalities: "**contacts**" should have been **contact** in line 4. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Vaiyapuri et al. (US 6,207,467 B1).

Vaiyapuri et al. teaches a substrate 12 in an integrated circuit (IC) package **100**, comprising: opposing first and second surfaces, wherein one of the first and the second surfaces has a plurality of solder ball contact pads **39** formed thereon, wherein the first surface has a central opening, wherein the central opening has an edge, wherein the edge includes at least one protruding edge portion 28 that extends into the central opening, whereby the at least one protruding edge portion provides a shorter distance between a trace (connected to 33) on the first surface and an IC die 18 relative to a distance between the trace and the IC die when the at least one protruding edge portion is not present, wherein the central opening being substantially rectangular; ball grid array IC package; at least one protruding edge portion being tab-shaped; a trace on the first surface corresponding to the at least one protruding edge portion, wherein the trace extending into the at least one protruding edge portion; and the at least one protruding edge portion being configured to allow a wire 20 to couple an IC die to the trace (Figure 2, col. 2, lines 19-55).

Claims 8-9, 11-12, 22-25, 32, 35, 47-48 and 53-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Siu (US 6,664,617 B2).

In regard to claim 8, Siu teaches a substrate 130 in an integrated circuit (IC) package, comprising: opposing first and second surfaces, wherein one of the first and the second surfaces has a plurality of solder ball contact pads 320 formed thereon, wherein the first surface has a central opening, wherein the central opening has an

edge, wherein the edge includes at least one recessed edge portion, whereby the at least one recessed edge portion provides access to a portion of a surface of a stiffener 120 attached to the substrate 130 relative to when the at least one recessed edge portion is not present (Figures 2B-2C and 3B, cols. 5-6, lines 7-67 and 1-24, respectively).

In regard to claim 9, 11-12 and 16-17, Siu teaches the substrate capable of being coupled to a surface of a stiffener that has a central bonding ring 114, where the at least one recessed edge portion configured to expose a portion of the central bondable ring when the substrate is coupled to the stiffener surface; substantially rectangular central opening; and a ball grid array IC package (Figure 3B, col. 5, lines 53-59).

In regard to claim 25, Siu teaches the first surface of the stiffener 120 having a central cavity that coincides with the central opening of the substrate 130, wherein the central bondable ring 114 surrounds the central cavity (Figure 3B).

In regard to claims 32 and 35, Siu teaches a ground central bondable ring (Figure 3B, cols. 4 and 5, lines 8-16 and 53-59, respectively).

In regard to claims 47-48 and 53-54, Siu teaches plurality of solder ball contact pads on the first and second surfaces of the substrate 40 (on the top right-hand side of the structure) (Figures 4C and 4D).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 18-21, 26-27, 34, 39-41 and 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siu (US 6,664,617 B2) as applied to claims 8-9, 11-12, 22-25, 32, 35, 47-48 and 53-54 above, and further in view of Zhang et al. (US 2002/0171144 A1).

Siu teaches all mentioned in the rejection above. In regard to claim 10, Siu further teaches the at least one recessed edge portion configures to allow a corresponding bond wire 50 to couple an IC die 40 to the central bonding ring 114 (Figures 2B-2C and 3B, col. 5, lines 7-59). In regard to claim 18, Siu further teaches the first portion of the edge configured to cover a first portion of the central bondable ring when the substrate is coupled to the surface of the stiffener, and the second portion of the edge configured to expose a second portion of the central bondable ring when the substrate is coupled to the surface of the stiffener (Figure 3B). In regard to claim 19, Siu further teaches the second portion of the edge configured to allow a wire 50 to couple an IC die 40 to the second portion of the central bondable ring (Figure 3B). In regard to claims 40-41, Siu further teaches bond wires 50 (right-hand side wires) that couples a pin of the IC die 40 to the trace on the first surface of the substrate proximate to the edge and the portion of central bondable ring exposed by the recessed edge portion (Figures 2C and 3B).

However, Siu fails to teach an IC die mounted on the surface of the stiffener; and a first trace on the first surface of the substrate proximate to a first portion of the edge; a

second on the first surface of the substrate proximate to a second portion of the edge, whereby the first portion of the edge allows for a shorter distance between the first trance and an IC die relative to a distance between the second trace and the IC die.

In regard to claims 10 and 26-27, Zhang et al. teach an IC die 102 mounted on the surface of the stiffener 304; an IC die 102 attached to the first surface of the stiffener 304 in the central cavity; and the IC die attached to the first surface of the stiffener within the central opening of the first surface of the substrate (Figure 3, page 3, paragraph [0052]).

In regard to claim 18, Zhang et al. teach a first trace on the first surface of the substrate 402 proximate to a first portion of the edge (the center portion of Figure 4 of Zhang et al. has several edge portions and various traces leading to/from the center portion); a second on the first surface of the substrate proximate to a second portion of the edge, whereby the first portion of the edge allows for a shorter distance between the first trance and an IC die relative to a distance between the second trace and the IC die (Figure 4, page 3, paragraph [0051]).

Since Siu and Zhang et al. are from the same field of endeavor (integrated circuit (IC) packages having stiffeners), the purpose disclosed by Zhang et al. would have been pertinent in the art of Siu. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the substrate in an integrated circuit (IC) package as taught by Siu with the substrate in an integrated circuit (IC) package having an IC die mounted on the surface of the stiffener as taught by Zhang et al. to aid in the spreading of heat from the IC die (page 3, paragraph [0052]).

Claims 13 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siu (US 6,664,617 B2) as applied to claims 8-9, 11-12, 22-25, 32, 35, 47-48 and 53-54 above, and further in view of Lau et al. (6,057,601).

Siu and Zhang et al. teach all mentioned in the rejection above. However, Siu and Zhang et al. fail to teach the first surface including at least one hole proximate to the edge, whereby the at least one hole proximate to the edge provides access to a portion of a surface of a stiffener attached to the substrate relative to when the at least one hole proximate to the edge is not present. Lau et al. teach the first surface including at least one hole 187 proximate to an edge, whereby the at least one hole proximate to the edge provides access to a portion of a surface of a stiffener attached to the substrate relative to when the at least one hole proximate to the edge is not present (Figure 3A, cols. 6-7, lines 21-67 and 1-22, respectively). Since Siu and Lau et al. are from the same field of endeavor (integrated circuit (IC) packages having stiffeners), the purpose disclosed by Lau et al. would have been pertinent in the art of Siu. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the substrate in an integrated circuit (IC) package as taught by Siu with the substrate in an integrated circuit (IC) package having a hole proximate the edge as taught by Lau et al. to provide a less complicated manufacture method such that the production yields and product reliability are improved (col. 3, lines 44-50).

Claims 2, 31, 36-38 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siu (US 6,664,617 B2) and Zhang et al. (US 2002/0171144 A1) as applied to claims 1, 3-12, 18-27, 32, 34-35, 39-41, 47-48 and 51-54 above, and further in view of Vaiyapuri et al. (US 6,207,467 B1).

Siu and Zhang et al. teach all mentioned in the rejection above. In regard to claims 37-38, Siu further teaches bond wires 50 (right-hand side wires) that couples a pin of the IC die 40 to the trace and the central bondable ring (Figures 2C and 3B). However, Siu and Zhang et al. fail to teach the edge having a protruding edge portion that extends across a portion of the central bondable ring, wherein a trace on the first surface of the substrate extends into the protruding edge portion; whereby the protruding edge portion provides a shorter distance between the trace and the IC die relative a distance between the trace and the IC die when the protruding edge is not present. Vaiyapuri et al. teach the edge having a protruding edge portion 28 that extends into the central opening, whereby the at least one protruding edge portion provides a shorter distance between a trace (connected to 33) on the first surface and an IC die 18 relative to a distance between the trace and the IC die when the at least one protruding edge portion is not present (Figure 2, col. 2, lines 19-55). Since Siu, Zhang et al. and Vaiyapuri et al. are from the same field of endeavor (integrated circuit (IC) packages), the purpose disclosed by Vaiyapuri et al. would have been pertinent in the art of Siu and Zhang et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the substrate in an integrated circuit (IC) package as taught by Siu and the substrate in an integrated circuit (IC) package having an IC die

mounted on the surface of the stiffener as taught by Zhang et al. with the substrate in an integrated circuit (IC) package having a protruding edge portion as taught by Vaiyapuri et al. to provide to capability to develop multi-chip structures (col. 1, lines 7-17).

Claims 14-15, 33, 42-44 and 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siu (US 6,664,617 B2) and Zhang et al. (US 2002/0171144 A1) as applied to claims 1, 3-12, 18-27, 32, 34-35, 39-41, 47-48 and 51-54 above, and further in view of Lau et al. (6,057,601).

Siu and Zhang et al. teach all mentioned in the rejection above. In regard to claim 43, Siu further teaches bond wire 50 (right-hand side wires) that couples a pin of the IC die 40 to the trace on the first surface of the substrate proximate to the edge and to the portion of the central bondable ring (Figures 2C and 3B). However, Siu and Zhang et al. fail to teach the first surface of the substrate having a hole proximate to an edge of the central opening; and at least one hole configured to allow a corresponding bond wire to couple an IC die mounted on the surface of the stiffener. Lau et al. teach the first surface of the substrate 105 having a hole 187 proximate to an edge of the central opening; and at least one hole 187 configured to allow a corresponding bond wire 170 to couple an IC die 125 mounted on the surface of the stiffener 106 -(Figure 3A, cols. 6-7, lines 21-67 and 1-22, respectively). In regard to claim 44, Lau et al. further teach a bond wire 170 that couples a pin of the IC die (Figures 2C and 3B). Since Siu, Zhang et al. and Lau et al. are from the same field of endeavor (integrated circuit (IC) packages having stiffeners), the purpose disclosed by Lau et al. would have

been pertinent in the art of Siu and Zhang et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the substrate in an integrated circuit (IC) package as taught by Siu and the substrate in an integrated circuit (IC) package having an IC die mounted on the surface of the stiffener as taught by Zhang et al. with the holes in the substrate proximate the edge of the central opening as taught by Lau et al. to provide a new semiconductor device package assembly supported on an improved heat spreader provided with a substrate placement recess (col. 4, lines 13-23).

Response to Arguments

Applicant's arguments with respect to claims 1-27 and 31-54 have been considered but are moot in view of the newly applied reference.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent are cited to further show the state of the art with respects to integrated circuit package structures:

Edwards et al. (5,650,662)	Eghan et al. (US 2002/0185717 A1)
Fernandez et al. (US 6,278,613 B1)	Glenn et al. (US 6,528,869 B1)
Sasano (US 6,313,525 B1)	Schueller et al. (US 2001/0001505 A1)
Stearns et al. (5,895,967)	Toshio et al. (US 6,617,193 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
February 20, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800